Single Mode Bluetooth Low Energy (BLE) Module

Part # BL600-SA, BL600-SC, BL600-ST

Hardware Integration Guide

Version 1.0

global solutions: local support

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www.lairdtech.com/wireless

REVISION HISTORY

Version	Revision Date	Change History
Version 1.0	16April13	Initial Release

CONTENTS

1 Overview and Key Features

Every BL600 Series module is designed to enable OEMs to add single-mode Bluetooth Low Energy (BLE) to small, portable, power –conscious devices. The BL600 modules are enabled with Laird's *smart*BASIC, an event-driven programming language that enables OEMs to make their BLE product development quicker, and simpler, significantly reducing time to market. *smart*BASIC enables customers to develop a complete embedded application inside the compact BL600 hardware, connecting to a wide array of external sensors via its I2C, SPI, UART, ADC or GPIO interfaces.

Based on the world-leading Nordic Semiconductor nRF51822 chipset, the BL600 modules provide ultra-low power consumption with outstanding wireless range via 4dBm of transmit power. A broad range of BLE profiles including Temperature and Heart Rate are available and *smart*BASIC provides the ideal mechanism to support any BLE profile development of your choice.

Features & Benefits

- Bluetooth v4.0 - Single Mode
- External or Internal Antennas
- *smart*BASIC programming language
- Full Bluetooth EPL
- Compact Footprint
- Programmable TX power 4 dBm to -20 dBm
- TX whisper mode (-30 dBm, -55 dBm)
- RX sensitivity: -91 dBm
- Ultra low power consumption
- TX: 11.6 mA peak (at +4 dBm)
- RX: 8.8 mA peak
- Standby Doze: 3.5 uA
- Deep Sleep: 0.4 uA (refer to Note4 in Power Consumption section)
- UART, GPIO, ADC, I2C, and SPI interfaces
- Fast Time to Market
- FCC, CE, IC, and Japan certified; other regulatory certifications on request
- No external components required

Application Areas

- Medical devices
- Wellness devices
- iOS "appcessories"
- Fitness sensors
- Location Awareness
- Home automation

2 SPECIFICATION

2.1 Specification Summary

Table 1: Specifications

Categories	Feature	Implementation
Wireless Specification	Bluetooth®	V4.0 – Single Mode Slave (in base FW v1.1.50.0)
	Frequency	2.402 - 2.480 GHz
	Maximum Transmit Power Setting	4 dBm Conducted BL600-SA 4 dBm Conducted BL600-SC ~2.5 dBm Conducted BL600-ST (RSMA connector on dev board)
	Minimum Transmit Power Setting	-20 dBm (in 4 dB steps) with *smart*BASIC command -16 dBm -12 dBm - 8 dBm - 4 dBm 0 dBm
	TX Whisper Mode1 Transmit Power	-30 dBm (min) with *smart*BASIC command
	TX Whisper Mode2 Transmit Power	-55 dBm (min) with *smart*BASIC command
	Receive Sensitivity (0.1% BER)	-91 dBm typical
	Link Budget	95 dB (@ 1 Mbps)
	Range	Up to 150 m in free space
	TX Whisper Modes	Range reduction feature with TX Whisper Modes with *smart*BASIC command.
	Range (TX Whisper Mode2)	~30 cm
	Raw Data Rates	1 Mbps (over the air)
Host Interface	TOTAL	28 x Multifunction I/O lines
	UART	TX, RX, CTS, RTS DCD, RI, DTR, DSR, CTS, RTS (Note1) Default 9600, n,8, 1 From 1,200 to 115,200bps
	GPIO	Up to 28 lines
	ADC	6 lines 8, 9, 10 bit resolution 1.2 V internal reference 1/1, 2/3, 1/3 pre-scaling
	I2C	2 lines (Note2)

Categories	Feature	Implementation
	SPI	3 lines (Note 3)
Profiles	Services supported (Note 4) (FW v1.1.50.0)	▪ Heart Rate Service ▪ Health Thermometer Service ▪ Battery Alert Service ▪ Blood Pressure Service ▪ Device Information Service ▪ Immediate Alert Service ▪ IOPT (Interoperability) ▪ Link Loss Service ▪ Transmit Power Service
FW upgrade	*smart*BASIC runtime engine FW(Note5) upgrade	Via JTAG (until further notice). Using the supplied J-link programmer. Via UART (in future FW).
	*smart*BASIC application script upgrade	Via UART.
Programmability	*smart*BASIC	On-board Programming language similar to BASIC.
Control Protocols	Any	User defined via *smart*BASIC
Operating Modes	Self-contained Run mode:	Selected by nAutoRun pin status: LOW (0V). Then runs $autorun$ (*smart*BASIC application script) if it exists.
	Interactive / development mode:	HIGH (VCC). Then runs via at+run (and "file name" of *smart*BASIC application script).
Supply Voltage	Supply (VCC)	2.1 – 3.6 V – internal DCDC converter 1.8 – 3.6 V – internal LDO DCDC switched on if VCC>2.1V at power-up.
Power Consumption	Active Modes Peak Current (for Max TX PWR 4 dBm)	Advertising or Connected mode: 11.6 mA peak TX, 8.9 mA peak RX
	Active Modes Peak Current for TX Whisper mode2 PWR -55 dBm)	Advertising or Connected mode: 5 mA peak TX, 8.5 mA peak RX
	Active Modes Average Current	Depends on many factors, refer to section *Power Consumption*.
	Ultra Low Power Modes	Standby Doze: 3.5 uA Deep Sleep: 400 nA (Note 5)
Antenna Options	Internal	Ceramic chip monopole antenna – on-board **BL600-SA**
	External – Option 1	Dipole antenna (with IPEX connector) Dipole PCB antenna (with IPEX connector) Connection via IPEX MH4 – **BL600-SC**
	External – Option 2	Dipole antenna (with RSMA connector) Connection via Trace Pads – **BL600-ST**

Categories	Feature	Implementation
Physical	Dimensions	19 mm x 12.5 mm x 3 mm
	Weight	<1 gram
Environmental	Operating	-25 ˚C to +75 ˚C
	Storage	-40 ˚C to +85 ˚C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	1 Year
Development Tools	Development Kit	Development Kit DVK-BL600-Sx and Free Software Tools
Approvals	Bluetooth®	End Product Listing (EPL)
	FCC / IC / CE / MIC	All BL600 Series

Note 1: DSR, DTR, RI, and DCD can be implemented in *smart*BASIC Application.

Note 2: With I2C interface selected, pull-up resistors on I2C SDA and I2C SCL MUST be connected externally as per I2C standard.

Note 3: SPI CS is created by customer using any spare SIO pin within their *smart*BASIC application script allowing multi-dropping

Note 4: BL600 module comes loaded with *smart*BASIC runtime engine FW, but does not come loaded with any *smart*BASIC application script (as that is dependent on customer end application or use). Laird provides many sample *smart*BASIC application scripts covering the services listed. Additional BLE services being added every quarter.

Note 5: Current Nordic silicon ~1000nA (typical). In next silicon revision this figure is expected to be within specification (400nA).

3 HARDWARE SPECIFICATIONS

3.1 Block Diagram and Pin-out

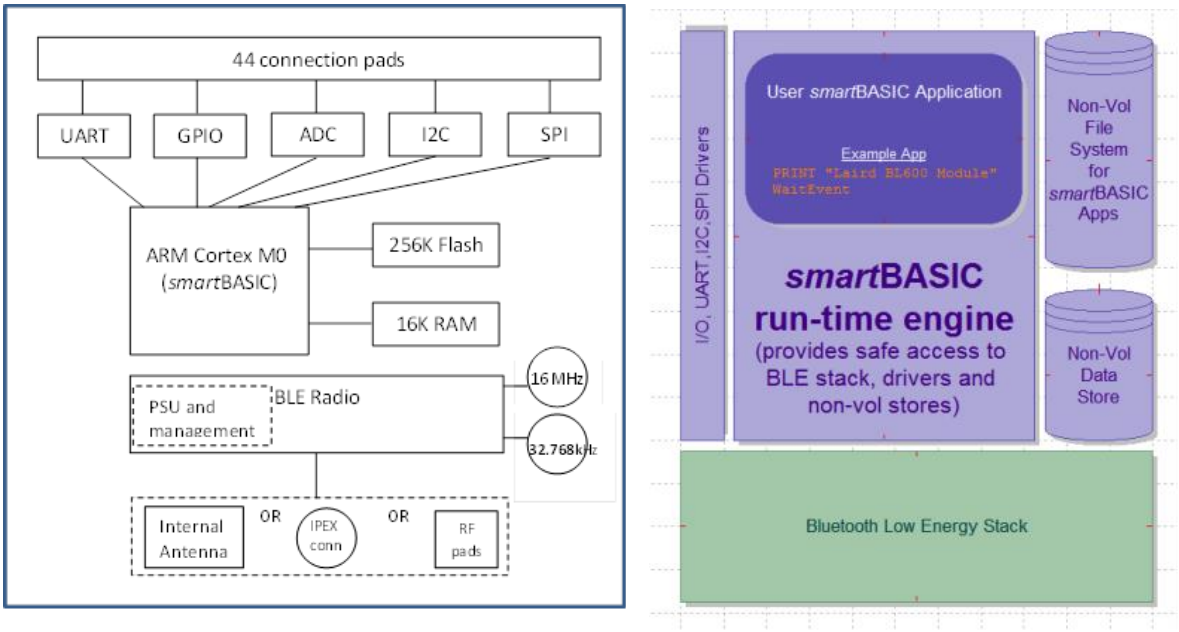


*Figure 1: Functional HW and SW block Diagram for BL600 series BLE smart*BASIC *module*

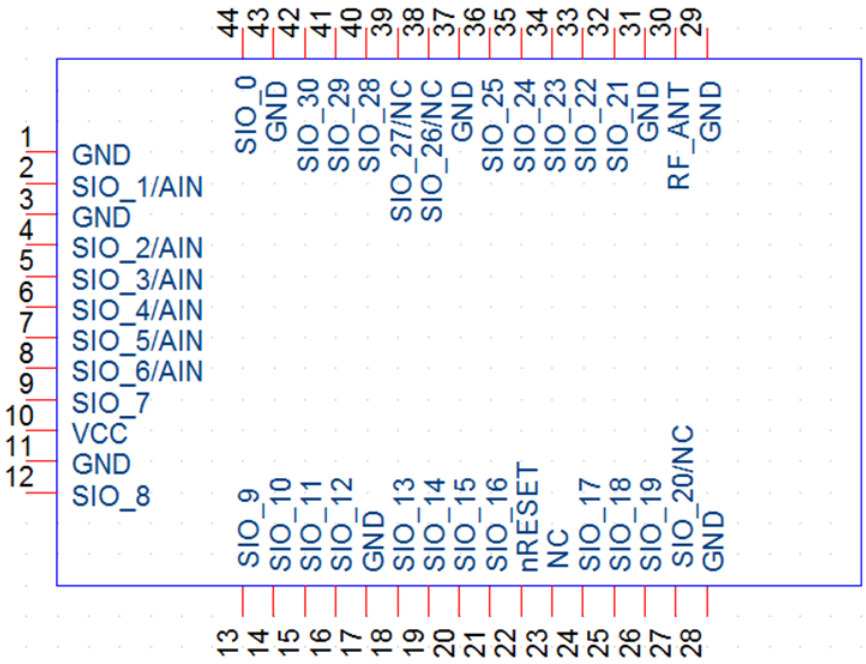


Figure 2: BL600-Sx module pin-out (top view).

Note: Pin 30 RF_ANT for BL600-ST only. On BL600-SA, BL600-SC, pin 30 is NC.

3.1 Pin Definitions

Table 2: Pin definitions

Pin #	Pin Designation	Default Function	Alternate Function	Default Direction	Notes	Comment
1	GND					
2	SIO_1	DIO	AIN	IN	1,2,3,4,5	8,9,10 bit resolution. Voltage scaling 1/1, 2/3, 1/3.
3	GND					
4	SIO_2	DIO	AIN	IN	1,2,3,4,5	8,9,10 bit resolution. Voltage scaling 1/1, 2/3, 1/3.
5	SIO_3	DIO	AIN	IN	1,2,3,4,5	8,9,10 bit resolution, Voltage scaling 1/1, 2/3, 1/3.
6	SIO_4	DIO	AIN	IN	1,2,3,4,5	8,9,10 bit resolution, Voltage scaling 1/1, 2/3, 1/3.
7	SIO_5	DIO	AIN	IN	1,2,3,4,5	8,9,10 bit resolution, Voltage scaling 1/1, 2/3, 1/3.
8	SIO_6	DIO	AIN	IN	1,2,3,4,5	8,9,10 bit resolution, Voltage scaling 1/1, 2/3, 1/3.
9	SIO_7	DIO		IN	1,2	
10	VCC					
11	GND					
12	SIO_8	DIO	I2C SDA	IN	1,2,4,5,6	I2COPEN() in *smart*BASIC selects I2C function
13	SIO_9	DIO	I2C SCL	IN	1,2,4,5,6	
14	SIO_10	DIO	SPI MOSI	IN	1,2,4,5,6	SPIOPEN() in *smart*BASIC selects SPI function, MOSI and CLK will be outputs when in SPI master mode. Note 11.
15	SIO_11	DIO	SPI MISO	IN	1,2,4,5,6	
16	SIO_12	DIO	SPI CLK	IN	1,2,4,5,6	
17	GND					
18	SIO_13	DIO		IN	1,2	
19	SIO_14	DIO		IN	1,2	
20	SIO_15	DIO		IN	1,2	Laird Devkit : Buzzer output
21	SIO_16	DIO		IN	1,2	Laird Devkit : Button 0 input
22	nRESET			IN	9,10	System Reset (Active low)
23	NC				9	DO NOT CONNECT
24	SIO_17	DIO		IN	1,2	Laird Devkit : Button 1 input
25	SIO_18	DIO		IN	1,2	Laird Devkit : LED 0
26	SIO_19	DIO		IN	1,2	Laird Devkit : LED 1
27	SIO_20	NC				Reserved for future use
28	GND					
29	GND					
30	RF_ANT				8	Used on BL600-ST only.
31	GND					
32	SIO_21	DIO	UART TX	OUT	1,2,4,6,7	UARTCLOSE() selects DIO

Pin #	Pin Designation	Default Function	Alternate Function	Default Direction	Notes	Comment
33	SIO_22	**DIO**	**UART RX**	IN	1,2,4,6,7	functionality and UARTOPEN() selects uart comms behaviour
34	SIO_23	**DIO**	**UART RTS**	OUT	1,2,4,6,7	
35	SIO_24	**DIO**	**UART CTS**	IN	1,2,4,6,7	
36	SIO_25	**DIO**		IN	1,2	Laird Devkit : UART_DTR via CON12
37	GND					
38	SIO_26	**NC**				Reserved for future use. Do NOT connect.
39	SIO_27	**NC**				
40	SIO_28	**nAutoRUN**		IN	In ONLY	Laird Devkit: UART_DSR via CON12
41	SIO_29	**DIO**		IN	1,2	Laird Devkit : UART_DCD via CON12
42	SIO_30	**DIO**		IN	1,2	Laird Devkit : UART_RI via CON12
43	GND					
44	SIO_0	**DIO**		IN	1,2	

Note 1: Secondary function is selectable in *smart*BASIC application.

Note 2: DIO = Digital Input or Output. I/O voltage level tracks VCC.

Note 3: AIN = Analog Input

Note 4: DIO or AIN functionality is selected using the GpioSetFunc() function in *smart*BASIC.

Note 5: AIN configuration selected using GpioSetFunc() function.

Note 6: I2C, UART, SPI controlled by xxxOPEN() functions in *smart*BASIC.

Note 7: SIO_21 to SIO_24 are DIO by default when $autorun$ app runs on power up.

Note 8: RF_ANT pin (pin30) is on theBL600-ST module only. Customer MUST use 50-Ohm trace from RF_ANT pin to RSMA RF connector on host PCB. More details on 50-Ohm trace design refer to section *50-OhmsRF Trace on Host PCB for BL600-ST*.

Note 9: Hidden JTAG (2-wire interface), pin22 (SWDIO) and pin23 (SWDCLK). Used for upgrading *smart*BASIC runtime engine FW only with Laird supplied J-link programmer. Using this hidden JTAG requires 12K resistor to GND (on pin23 SWDCLK) on customers host PCB and header connector Samtech FTSH-105-01-L-DV, refer to section *Miscellaneous (hidden JTAG)* for details.

Note 10: Pull the nRESET pin low for minimum 100 mS in order for the BL600 to reset.

Note11: SPI CS is created by customer using any spare SIO pin within their *smart*BASIC application script allowing multi-dropping.

The BL600 module is delivered with the integrated *smart*BASIC runtime engine FW loaded (but no onboard *smart*BASIC application script). Because of this, it starts up in AT command mode by default.

At reset, all SIO lines are configured as the defaults shown above.

SIO lines can be configured through *smart*BASIC Application script to be either inputs or outputs with weak or strong pull-ups or pull-downs. When an alternative SIO function is selected (such as I2C or SPI), the firmware

does not allow the setup of internal pull-up/pull-down. Therefore, when I2C interface is selected, pull-up resistors on I2C SDA and I2C SCL **MUST** be connected externally as per I2C standard.

All the SIO pins (with "default function" of "DIO" are inputs (with no internal pull-up or pull-down), apart from SIO_21 and SIO_23 which are outputs):

- SIO_21 (alternative function UART_TX) is an output, set high (in FW).
- SIO_23 (alternative function UART_RTS) is an output, set low (in FW).
- SIO_22 (alternative function UART_RX) is an input, set with internal weak pull-up (in FW).
- SIO_24 (alternative function UART_CTS) is an input, set with internal weak pull-down (in FW).

UART_RX, UART_TX, UART_CTS are 3.3 V level logic (if VCC is 3.3 V, i.e. SIO pin I/O levels track VCC). For example, when RX and TX are idle, they sit at 3.3 V (if VCC is 3.3 V). Conversely, for handshaking pins CTS and RTS at 0 v are treated as assertions.

Pin 40 (nAutoRUN) is an input, with active low logic. In the development kit (DVK-BL600-sx) it is connected so that the state is driven by the host's DTR output line. The nAutoRUN pin must be externally held high or low to select between the following two BL600 operating modes:

- Self-contained Run mode (nAutoRUN pin held at 0 V).
- Interactive / development mode (nAutoRUN pin held at VCC).

*smart*BASIC runtime engine firmware checks for the status of nAutoRUN during power-up or reset. If it is low and if there is a *smart*BASIC application script named **$autorun$** then the *smart*BASIC runtime engine FW executes the application script automatically; hence the name S*elf-contained Run Mode*.

3.1 Electrical Specifications

3.1.1 Absolute Maximum ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below; exceeding these values causes permanent damage.

Parameter	Min	Max	Unit
Voltage at VCC pin	-0.3	+3.6	V
Voltage at GND pin		0	V
Voltage at SIO pin	-0.3	VCC+0.3	V
Storage temperature	-40	+85	ºC

3.1.2 Recommended Operating Parameters

3.1.2.1 Power Supply

Parameter	Min	Typ	Max	Unit
VCC (with internal LDO)[1]	1.8	3	3.6	V
VCC (with internal DCDC enabled)[1]	2.1	3	3.6	V
VCC Maximum ripple or noise[2]			10	mV
VCC rise time (0 to 1.8V)[3]			60	mS
Operating Temperature Range	-25	25	+75	ºC

Note 1: Internal DCDC is used if VCC >2.1 V on power-up; otherwise internal LDO is used. 4.7 uF internal to module on VCC.

Note 2: The maximum VCC ripple or noise (at any frequency) that does not disturb the radio.

Note 3: The on-board power-on reset circuitry may not work properly for rise times outside the noted interval.
Time reset is active from VCC reaches 1.7 V with 50 mS rise time is 29 mS typical.
Time reset is active from VCC reaches 1.7 V with 1 uS rise time is 2.7 uS typical.

3.1.2.2 Signal Levels for Interface, SIO

Parameter	Min	Typ	Max	Unit
VIH Input high voltage	0.7VCC		VCC	V
VIL Input low voltage	VSS		3.6	V
VOH Output high voltage				
(std. drive, 0.5mA)	VCC-0.3		VCC	V
(high-drive, 5mA)[1] Note 2	VCC-0.3		VCC	V
VOL Output low voltage				
(std. drive, 0.5mA)	VSS		0.3	V
(high-drive, 5mA)[1]	VSS		0.3	V
Pull up resistance	11	13	16	kΩ
Pull down resistance	11	13	16	kΩ

Note 1: Maximum number of pins with 5 mA high drive is three.

3.1.2.3 SIO pin alternative function AIN (ADC) specification

Parameter	Min	Typ	Max	Unit
ADC Internal reference voltage	-1.5%	1.2 V	+1.5%	%
ADC pin input internal selectable scaling		1/1 1/3 2/3		scaling
ADC input pin (AIN) voltage maximum without damaging ADC w.r.t VCC Prescaling				
3.6 V 1/1			2.4	V
3.6 V 2/3			3.6	V
3.6 V 1/3			3.6	V
3.3 V 1/1			2.4	V
3.3 V 2/3			3.6	V
3.3 V 1/3			3.6	V
1.8 V 1/1			2.1	V
1.8 V 2/3			2.1	V
1.8 V 1/3			2.1	V

Parameter	Min	Typ	Max	Unit
ADC input pin (AIN) voltage maximum without saturating ADC (with 1.2V internal reference)[1]				V
1/1 prescaling			1.2	V
2/3 prescaling			1.8	V
1/3 prescaling			3.6	
Time required to convert single sample in				
10bit mode				uS
9bit mode[2]		68		uS
8bit mode[2]		36		uS
		20		

Note 1: Stay within internal 1.2 V reference voltage with given prescaling on AIN pin and do not violate ADC maximum input voltage (for damage) for a given VCC, e.g. If VCC is 1.8 V can only expose AIN pin to 2.1 V (VCC+0.3).

Note 2: Current production *smart*BASIC runtime engine firmware (v1.1.50.0) allows only 10-bit mode.

3.1.3 nAutoRUN pin and Operating Modes

Operating modes (refer *smart*BASIC manual for details):

- Self-contained mode
- Interactive / Development mode

Signal Name	Pin No	I/O	Comments
nAutoRUN (SIO_28)	28	I	Input with active low logic. Operating mode selected by nAutoRun pin status: Low (0V), then runs $autorun$ if it exists; High (VCC) then run via at+run (and "file name" of *smart* BASIC application.

Pin 40 (nAutoRUN) is an input, with active low logic. In the development board (DVK-BL600-sx) it is connected so that the state is driven by the host's DTR output line. nAutoRUN pin needs to be externally held high or low to select between the two BL600 operating modes:

- Self-contained Run mode (nAutoRUN pin held at 0V).
- Interactive / Development mode (nAutoRUN pin held at VCC).

*smart*BASIC runtime engine firmware checks for the status of nAutoRUN during power-up or reset. If it is low and if there is a *smart*BASIC application named $autorun$ then the *smart*BASIC runtime engine executes the application automatically; hence the name *self-contained run mode*.

4 POWER CONSUMPTION

Data taken at VCC 3.3V (internal DCDC convertor ON) and 25ºC.

4.1 Power Consumption

Parameter	Min	Typ	Max	Unit
Active mode 'peak' current **–Note1**				
(Advertising or Connection)				mA
TX only run peak current @TXpwr= +4 dBm		11.6		mA
TX only run peak current @T pwr= 0 dBm		8.4		mA
TX only run peak current @TXpwr= -4 dBm		7.1		mA
TX only run peak current @TXpwr= -8 dBm		6.9		mA
TX only run peak current @TXpwr= -12 dBm		6.4		mA
TX only run peak current @TXpwr= -16 dBm		6.1		mA
T X only run peak current @TXpwr= -20 dBm		5.5		
TX Whisper mode 1(Note2)				mA
TX only run peak current @TXpwr= -30 dBm		5.4		
TX Whisper mode 2(Note2)				
TX only run peak current @TXpwr= -55 dBm		5.0		
Active Mode				
RX only 'peak' current(Note2)		8.9		mA
Ultra Low Power Mode1(Note3)				
Standby Doze		3.5		uA
Ultra Low Power Mode2(Note4)				
Deep Sleep (no RAM retention)		400 (Note 4)		nA
Active Mode Average current (Note5)				
Advertising Average Current draw				
Max, with advertising interval (min) 20 mS		~800		uA
Min, with advertising interval (max) 10240 mS		~4.1		uA
Connection Average Current draw				
Max, with connection interval (min) 7.5 mS				uA
with connection interval 67.5 mS		~400		uA
Min, with connection interval (max) 4000 mS		~4.1		uA

Note1: With VCC 3.3V (internal DCDC ON). If VCC reduces to 2.1V (operating range of DCDC, the peak current consumption would increase from 11.6mA to ~15.5mA for TX power setting of +4dBm.

Note2: Firmware version 1.1.50.0 (only) has an issue that TX PWR settings need to -40 dBm to produce -30 dBm and -65 dBm to produce -55 dBm.

Note3: Standby Doze is entered automatically (when *waitevent* statement is encountered within a *smart*BASIC application script). In Standby Doze, all peripherals that are enabled stay on and may re-awaken the chip. Depending on active peripherals, current consumption ranges from ~2-4 µA to > 1 mA. See individual peripherals current consumption in tables in section *Peripheral block current consumption 4.3*.

Note 4: In Deep Sleep, everything is disabled and the only wake-up sources are reset and changed on pins on which sense is enabled. The current consumption seen is ~1000 nA typical. In next silicon revision this figure is expected to be within specification (400nA). Current *smart*BASIC runtime engine firmware (v1.1.50.0) allows coming out of deep sleep through HW reset only. Future firmware releases allow coming out from Deep Sleep to Standby Doze through GPIO signal through the reset vector. Deep Sleep mode is entered (with a command in *smart*BASIC application script).

Note 5: Data taken with TX power 4 dBm and all peripherals off (UART OFF after radio event), slave latency of 0 (in a connection).
Average current consumption depends on a number of factors [including TX power, VCC accuracy of 16 MHz and 32.768 kHz). With these factors fixed, the largest variable is the advertising or connection interval set.

Advertising Interval range:
20 ms to 10240 ms in multiples of 0.625 ms for Advert type=ADV_IND and ADV_DIRECT_IND.
100 ms to 10240 ms in multiples of 0.625 ms for Advert type=ADV_SCAN_IND and ADV_NONCONN_IND.
For advertising timeout, if the advert type is ADV_DIRECT_IND, then the timeout is limited to 1.28 seconds (1280 ms).

For an advertising event,
- the minimum average current consumption is when the advertising interval is large 10240 mS (although this may cause long discover times (for the advertising event) by scanners.
- the maximum average current consumption is when the advertising interval is small 20 mS.
Other factors that are also related to average current consumption include the advertising payload bytes in each advertising packet and whether continuously advertising or periodically advertising.

Connection Interval range: 7.5 ms
to 4000 ms in multiples of 1.25 ms.

For a connection event,
- the minimum average current consumption is when the connection interval is large 4000 mS.
– the maximum average current consumption is with the shortest connection interval of 7.5 ms; no slave latency.
Other factors that are also related to average current consumption include whether transmitting 6 packets per connection interval & each packet contains 20 bytes (which is the maximum for each packet) and an inaccurate 32 kHz master clock accuracy would increase the average current consumption.

4.2 Measured peak current waveforms during advertising and connection

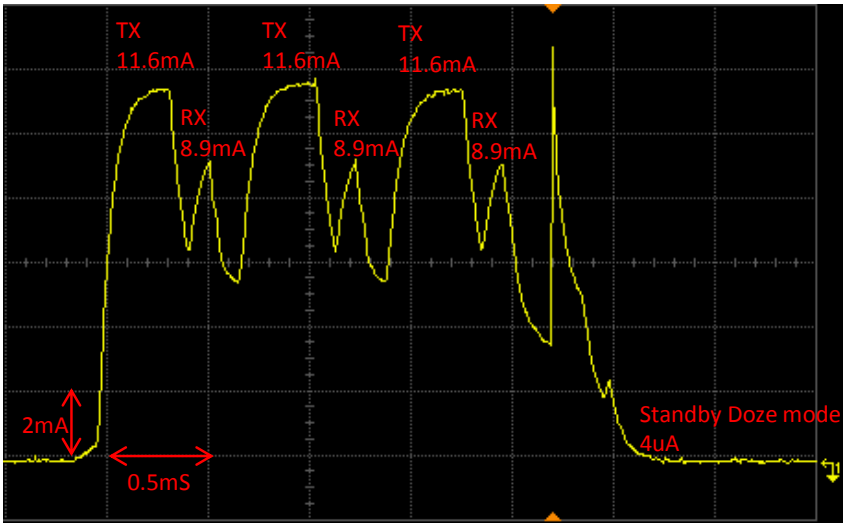


Figure 3: Typical peak current consumption profile during advertising in slave mode @ TX PWR +4dBm. UART is OFF. Last spike is DCDC being turned off.

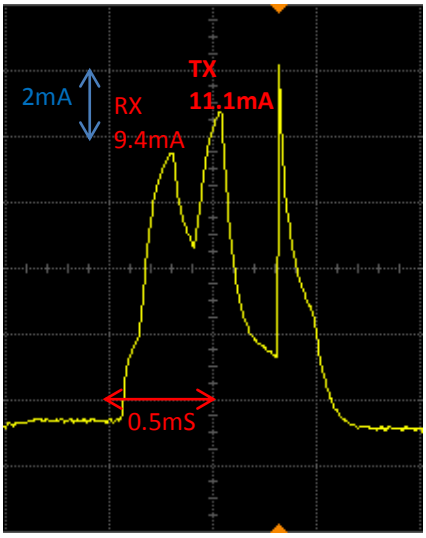
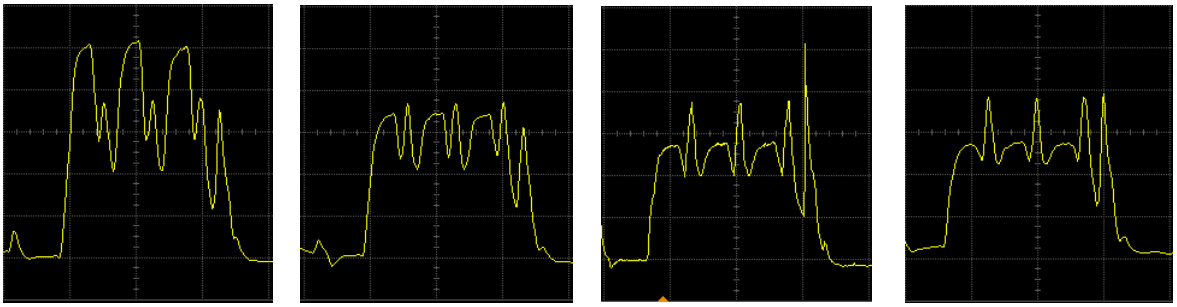


Figure 4: Typical peak current consumption profile during data connection event in slave mode @ TX PWR +4dBm. UART is ON. Last spike is DCDC being turned off.

4 dBm 0 dBm -4 dBm -8 dBm



-12 dBm -16 dBm -20 dBm

Figure 5: Typical peak current consumption profile during advertising in slave mode versus TX PWR

Advertising (with Whisper Mode TX powers)

-30dBm -55dBm

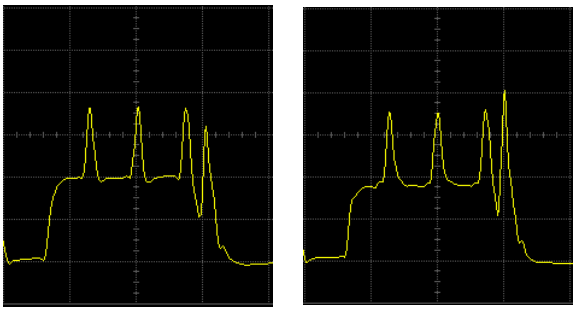


Figure 6: Typical peak current consumption profile during advertising in slave mode with TX Whisper Mode TX PWR -30 dBm (TX Whisper Mode1) and -55 dBm (TX Whisper Mode2).

Note: In the above pictures, UART is ON. X-axis time (1 mS per square), Y-axis current (2 mA per square).

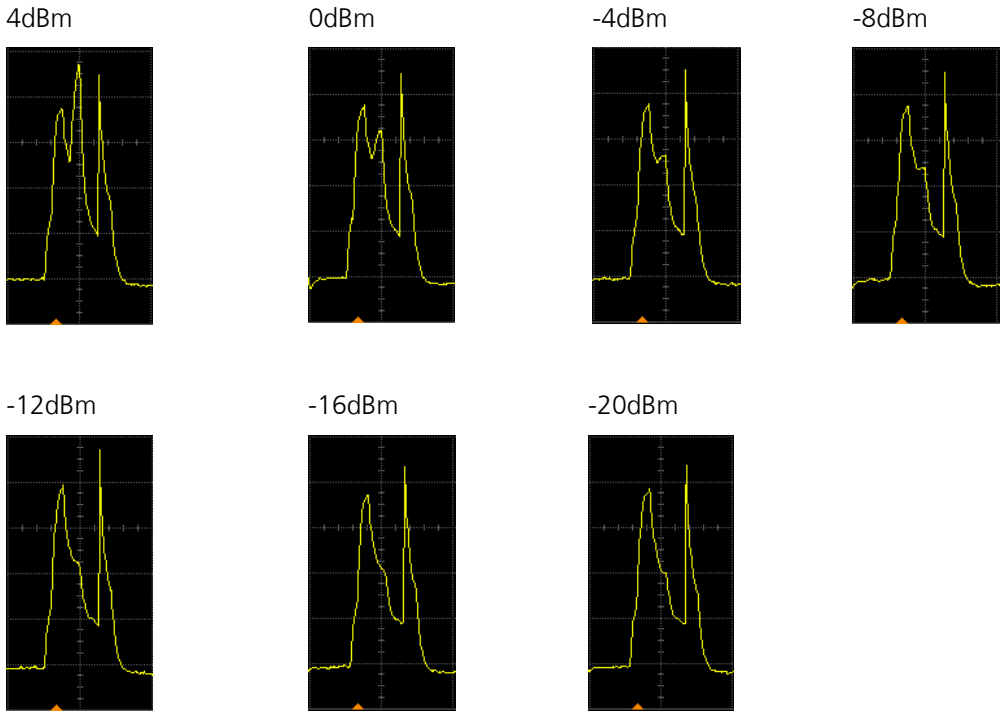


Figure 7: Typical peak current consumption profile during connection event in slave mode versus TX PWR.

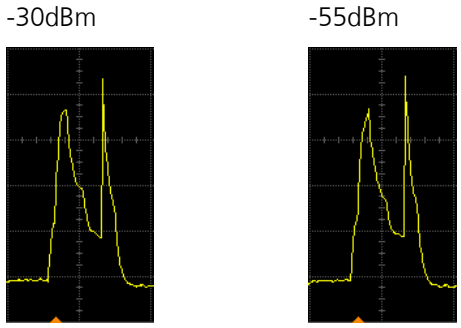


Figure 8: Typical peak current consumption profile during connection event in slave mode with TX Whisper mode TX PWR -30 dBm (TX Whisper Mode1) and -55 dBm (TX Whisper Mode2).

Note: In the above pictures, UART is ON. X-axis time (1 mS per square), Y-axis current (2 mA per square).

4.3 Peripheral block current consumption

The values below are calculated for a typical operating voltage of 3 V.

Table 3: UART Power Consumption

Parameter	Min	Typ	Max	Unit
UART Run current @ 115200 bps		220		uA
UART Run current @ 1200 bps		210		uA
UART Baud rate	1.2		115.2	kbps

Table 4: SPI Power Consumption

Parameter	Min	Typ	Max	Unit
SPI Master Run current @ 125 kbps		180		uA
SPI Master Run current @ 8 Mbps		220		uA
SPI bit rate	0.125		8	Mbps

Table 5: I2C Power Consumption

Parameter	Min	Typ	Max	Unit
I2C Run current @ 100 kbps		380		uA
I2C Run current @ 400 bps		400		uA
I2C Bit rate	100		400	kbps

Table 6: ADC

Parameter	Min	Typ	Max	Unit
ADC current during conversion		290		uA

The above current consumption is for the particular peripheral only and to operate that peripheral requires some other internal blocks which consume fixed amount of base current (~740uA). Current Nordic silicon this fixed base current is bit higher (by ~400uA).

This base current of ~1140 uA (= ~740uA+400uA) is consumed when the UART, SPI, I2C, or ADC is opened (operated).

For asynchronous interface like the UART (asynchronous as the other end can communicate at any time), the UART (on BL600) must kept open (by a command in *smart*BASIC application script) resulting in the base current consumption penalty.

For synchronous interface like the I2C or SPI (since BL600 side is the master), the interface can be closed and opened only (by a command in *smart*BASIC application script) when needed, resulting in current saving (no base current consumption penalty). Similar argument for ADC (open ADC when needed).

5 FUNCTIONAL DESCRIPTION

The BL600 BLE module is a self-contained Bluetooth Low Energy product and requires only power and a user's *smart*BASIC application to implement full BLE functionality. The integrated, high performance antenna combined with the RF and Base-band circuitry provides the Bluetooth Low Energy wireless link, and any of the SIO lines provide the OEM's chosen interface connection to the sensors. The user's *smart*BASIC application binds the sensors to the BLE wireless functionality.

The variety of hardware interfaces and the *smart*BASIC programming language allow the BL600 module to serve a wide range of wireless applications, whilst reducing overall time to market and the learning curve for developing BLE products.

To provide the widest scope for integration a variety of physical host interfaces / sensors are provided. The major BL600 series module functional blocks described below.

5.1 Power management (includes brown-out and power on reset)

Power management features:

- System Standby Doze / Deep Sleep modes.
- Brownout Reset.
- Open /Close Peripherals (UART, SPI, I2C, SIO's and ADC). Peripherals consume current when open; each peripheral can be individually closed to save power consumption (with a command in *a smart*BASIC application script).
- 2-region RAM retention (No RAM retention in Deep Sleep mode).
- Enable DCDC on power-up if VCC is >2.1V.
- *smart*BASIC command allows the VCC voltage to be read (through the internal ADC).
- Power fail comparator (in future FW).
- Pin wake-up system from Deep sleep (in future FW).

Power supply features:

- Supervisor HW to manage power on reset, brownout (and power fail).
- 1.8V to 3.6V supply range using internal LDO regulator.
- 2.1 to 3.6V supply range using internal DCDC convertor.
- The DCDC convertor can be disabled when supply voltage drops to below 2.1V so LDO can be used for low supply voltages (in future FW). When enabled, DCDC operation automatically suspended when only the internal low current LDO is needed.

This feature is useful for applications using battery technologies with higher nominal cell voltages. The reduction in supply voltage level from a high voltage to a low voltage reduces the peak power drain from the battery. Used with a 3 V coin-cell battery, the peak current drawn from the battery is reduced by approximately 30% (with DCDC enabled).

5.2 Clocks

The integrated high accuracy (+/-10ppm) 32.768kHz crystal oscillator provides protocol timing and helps with Radio power consumption in the system Standby Doze /Deep sleep modes by reducing the time that the RX window needs to be open. Standard accuracy clocks tend to have lower accuracy +/-250 ppm.

The integrated high accuracy 16 MHz crystal oscillator helps with Radio operation and also helps reduce power consumption in the Active modes.

5.3 Memory for *smart*BASIC application code

User has up to 4Kbytes of data memory available for *smart*BASIC application script.

5.4 RF

- 2402–2480MHz Bluetooth Low Energy radio (1Mbps over the air data rate).
- TX output power of +4dBm programmable (via *smart*BASIC command) to -20dBm in steps of 4dB.
- TX Whisper mode1 -30dBm (via *smart*BASIC command).
- TX Whisper mode2 -55dBm (via *smart*BASIC command).
- Receiver (with integrated channel filters) to achieve maximum sensitivity -91dBm @ 1Mbps BLE.
- RF conducted interface available in 3-ways:
  - BL600-SA - RF connected to on-board antenna on BL600-SA
  - BL600-SC -RF connected to on-board IPEX MH4 RF connector on BL600-SC
  - BL600-ST -RF connected to RF pad on BL600-ST.
- Antenna options:
  - Integrated monopole chip antenna on BL600-SA
  - External dipole antenna connected with to IPEX MH4 RF connector on BL600-SC.
  - External dipole antenna connected to RSMA RF connector which then is connected with 50-Ohms RF track on host PCB to RF pad on BL600-ST.

5.5 UART Interface

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control support (UART_CTS, UART_RTS) in HW up to 1 Mbps baud. Parity checking and generation for the 9th data bit are supported.

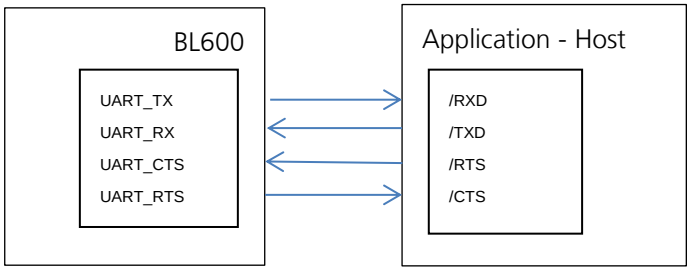
UART_TX, UART_RX, UART_RTS, and UART_CTS form a conventional asynchronous serial data port with handshaking. The interface is designed to operate correctly when connected to other UART devices such as the 16550A. The signalling levels are nominal 0 V and 3.3 V (tracks VCC) and are inverted with respect to the signalling on an RS232 cable.

Two-way hardware flow control is implemented by UART_RTS and UART_CTS. UART_RTS is an output and UART_CTS is an input. Both are active low.

These signals operate according to normal industry convention. UART_RX, UART_TX, UART_CTS, UART_RTS are all 3.3 V level logic (tracks VCC). For example, when RX and TX are idle they sit at 3.3 V. Conversely for handshaking pins CTS, RTS at 0 V is treated as an assertion.

The module communicates with the customer application using the following signals:

- Port /TXD of the application sends data to the module's UART_RX signal line
- Port /RXD of the application receives data from the module's UART_TX signal line



Note: The BL600 serial module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. Laird does not recommend linking CTS and RTS other than for testing and prototyping. If these pins are linked and the host sends data at the point that the BL600 deasserts its RTS signal, then there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This will drop the connection and may require a power cycle to reset the module. Laird recommends that the correct CTS/RTS handshaking protocol be adhered to for proper operation.

Table 7: UART Interface

Signal Name	Pin No	I/O	Comments
SIO_21 / UART_TX	32	O	SIO_21 (alternative function UART_TX) is an output, set high (in FW).
SIO_22 / UART_RX	33	I	SIO_22 (alternative function UART_RX) is an input, set with internal weak pull-up (in FW).
SIO_23 / UART_RTS	34	O	SIO_23 (alternative function UART_RTS) is an output, set low (in FW).
SIO_24 / UART_CTS	35	I	SIO_24 (alternative function UART_CTS) is an input, set with internal weak pull-down (in FW).

The UART interface is also used to load customer developed *smart*BASIC application script.

5.6 SPI Bus

The SPI interface is an alternate function on SIO pins, configurable by *smart*BASIC.

The Module is a master device that uses terminals SPI_MOSI, SPI_MISO, and SPI_CLK. SPI_CSB is implemented using any spare SIO digital output pins to allow for multi-dropping.

The SPI interface enables full duplex synchronous communication between devices. It supports a 3-wire (SPI_MOSI, SPI_MISO, SPI_SCK,) bidirectional bus with fast data transfers to and from multiple slaves. Individual chip select signals will be necessary for each of the slave devices attached to a bus, but control of these is left to the application through use of SIO signals. I/O data is double buffered.

The SPI peripheral supports SPI mode 0, 1, 2, and 3.

Signal Name	Pin No	I/O	Comments
SPI_MOSI	14	O	This interface is an alternate function configurable by *smart*BASIC. Default in the FW pin 14 and 16 are inputs. SPIOPEN() in *smart*BASIC selects SPI function and changes pin14 and 16 to outputs (when in SPI master mode).
SPI_MISO	15	I	
SPI_CLK	16	O	

5.7 I2C Interface

The I2C interface is an alternate function on SIO pins, configurable by *smart*BASIC command.

The Two-wire interface can interface a bi-directional wired-OR bus with two lines (SCL, SDA) and has master /slave topology. The interface is capable of clock stretching. Data rates of 100 kbps and 400 kbps are supported.

An I2C interface allows multiple masters and slaves to communicate over a shared wired-OR type bus consisting two lines which normally sit at VCC. The BL600 module can only be configured as an I2C master with additional constraint that it be the only master on the bus. The SCL is the clock line which is always sourced by the master and SDA is a bi-directional data line which can be driven by any device on the bus.

IMPORTANT: It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.

Table 8: I2C Interface

Signal Name	Pin No	I/O	Comments
I2C_SDA	12	I/O	This interface is an alternate function on each pin, configurable by *smart*BASIC. I2COPEN() in *smart*BASIC selects I2C function.
I2C_SCL	13	I/O	

5.8 General Purpose I/O, ADC and Quadrature Decoder

5.8.1 GPIO

The 28 SIO pins are configurable by *smart*BASIC. They can be accessed individually. Each has the following user configured features:

- Input/output direction
- Output drive strength (standard drive 0.5mA or high drive 5mA)
- Internal pull up and pull down resistors (13K typical) or no pull-up/down
- Wake-up from high or low level triggers on all pins

5.8.2 Quadrature Decoder

The following feature exists in hardware but cannot be configured in the firmware currently:

- The quadrature decoder provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors with an optional LED output signal and input debounce filters. The sample period and accumulation are configurable to match application requirements. All pins individually can be configured to carry quadrature demodulator signals.

5.8.3 ADC

The ADC is an alternate function on SIO pins, configurable by *smart*BASIC.

The BL600 provides access to six-channel 10-bit incremental ADC. This enables sampling up to six external signals through a front end MUX. The ADC has configurable input and reference prescaling and sample resolution (8, 9, and 10 bit).

Note: Current *smart*BASIC runtime engine firmware (v1.1.50.0) provides access to 10-bit mode resolution only. Future firmware will provide access to 8 and 9 bit resolution.

5.8.3.1 Analog Interface (ADC)

Signal Name	Pin No	I/O	Comments
AIN – Analog Input	2	I	This interface is an alternate function on each pin, configurable by *smart*BASIC. AIN configuration selected using GpioSetFunc() function. 8, 9, 10 bit resolution. Voltage scaling 1/1, 2/3, 1/3.
AIN – Analog Input	4	I	
AIN – Analog Input	5	I	
AIN – Analog Input	6	I	
AIN – Analog Input	7	I	
AIN – Analog Input	8	I	

5.9 nRESET pin

Signal Name	Pin No	I/O	Comments
nRESET	22	I	BL600 HW reset (active low). Pull the nRESET pin low for minimum 100mS in order for the BL600 to reset.

5.10 nAutoRUN pin

Refer to section *nAutoRUN pin and Operating Modes* regarding operating modes and the nAutoRUN pin.

- Self-contained Run mode
- Interactive / Development mode

5.11 Miscellaneous (Hidden JTAG)

The BL600 SW consists of:

- BL600 *smart*BASIC runtime engine FW (loaded at production, may be upgraded customer).
- BL600 *smart*BASIC application script developed by customer (loaded through UART by customer).

To allow customer the capability to upgrade the BL600 *smart*BASIC runtime engine FW, to the latest version released from Laird), the current *smart*BASIC runtime engine firmware (v1.1.50.0) only allows this upgrade via the hidden 2-wire (JTAG) interface. Future releases will support upgrading *smart*BASIC runtime engine FW over UART.

Signal Name (hidden name)	Pin No	I/O	Comments
nRESET (SWDIO)	22	I/O	
NC (SWDCLK)	23	I	Connect 12 K resistor to GND (for current silicon only).

Laird can supply JTAG J-link programmer for this.

Only requirement is that the customer should use the following JTAG connector on the host PCB.

The JTAG connector MPN is as follows:

Reference	Part	Description
JP1 Note1	FTSH-105	Header, 1.27mm, SMD, 10-way, FTSH-105-01-L-DV Samtech

Note 1: Reference on BL600 development board schematic. Figure 9 shows the BL600 development schematic wiring only for the JTAG connector and BL600 module hidden JTAG pins.

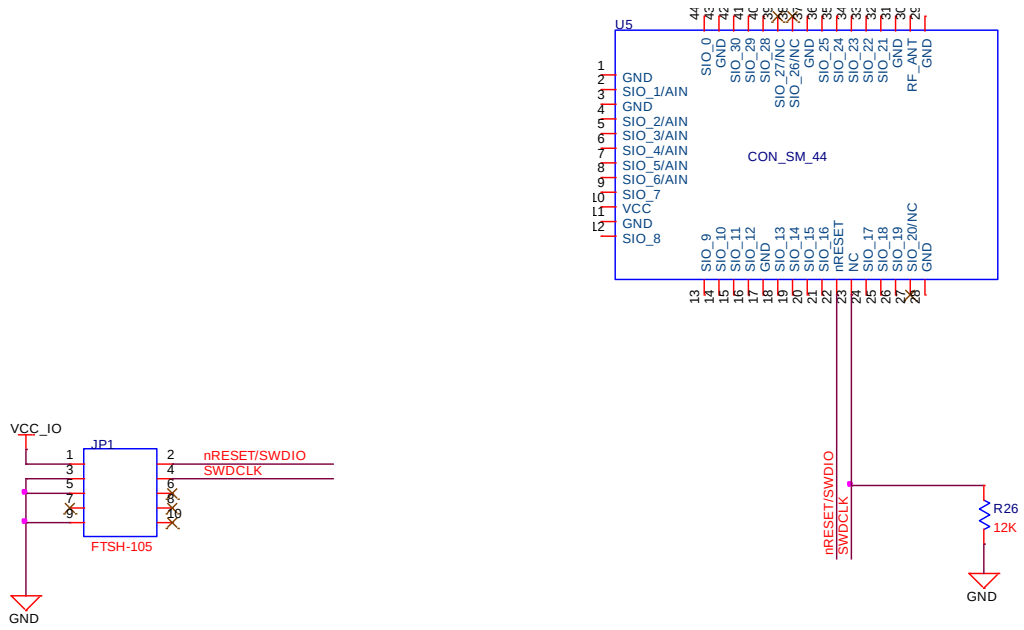


Figure 9: Wiring for JTAG connector to hidden JTAG on BL600 module

5.12 BL600-SA on-board chip antenna characteristics

The BL600-SA on-board chip monopole antenna radiated performance depends on the host PCB layout.

BL600 development board was used for BL600 development and antenna performance evaluation. To obtain similar performance follow guidelines in section *PCB Layout on Host PCB for BL600-SA* to allow the on-board antenna to radiate and reduce proximity effects due to nearby host PCB GND copper or metal covers.

BL600-SA on-board antenna datasheet:

http://www.acxc.com.tw/product/at5020/AT5020-E3R0HBAN_071204.pdf

6 HARDWARE INTEGRATION SUGGESTIONS

6.1 Circuit

The BL600-series module is easy to integrate requiring no external components on the customer's board apart from those required by customer for development and in customers end application.

Checklist (for Schematic)

- VCC
  External power source within the operating range, rise time and noise/ripple specification of BL600. Add decoupling capacitors for filtering the external source. Power-on reset circuitry within BL600 series module incorporates brown-out detector, thus simplifying power supply design. Upon application of power, the internal power-on reset ensures module starts correctly.
- VCC and coin-cell operation
  With built-in DCDC (operating range 2.1V to 3.6V), reduces the peak current required from a coin-cell (CR2032), making it easier to use with coin-cell.
- AIN (ADC) and SIO pin IO voltage levels
  BL600 SIO voltage levels are at VCC. Ensure input voltage levels into SIO pins are at VCC also (if VCC source is a battery whose voltage will drop). Ensure ADC pin maximum input voltage for damage is not violated.
- JTAG
  Is required if *smart*BASIC runtime engine FW upgrade capability is required (to upgrade to future /later releases from Laird), then add JTAG connector and 12K resistor to GND as detailed in section *Miscellaneous (hidden JTAG)*
- UART
  Is required for loading customer *smart*BASIC application script during development (or for subsequent upgrade). Add connector to allow UART to be interfaced to PC (via UART –RS232 or UART- USB).
- UART_RX and UART_CTS
  SIO_22 (alternative function UART_RX) is an input, set with internal weak pull-up (in FW). The pull-up prevents the module from going into deep sleep when UART_RX line is idling.

  SIO_24 (alternative function UART_CTS) is an input, set with internal weak pull-down (in FW). This pull-down ensures the default state of the UART_CTS will be asserted which means can send data out of the UART_TX line. In the case when UART_CTS is not connected (which we do not recommend).
- nAutoRUN pin and operating mode selection
  nAutoRUN pin needs to be externally held high or low to select between the two BL600 operating modes at power-up:
  - Self-contained Run mode (nAutoRUN pin held at 0V).
  - Interactive / development mode (nAutoRUN pin held at VCC).

  Make provision to allow operation in the required mode. Add jumper to allow nAutoRUN pin to be held high or low (via 10K resistor) OR driven by host GPIO.
- I2C
  It is essential to remember that pull-up resistors on both I2C_SCL and I2C_SDA lines are not provided in the BL600 module and MUST be provided external to the module as per I2C standard.

- SPI
  Implement SPI chip select using any unused SIO pin within your *smart*BASIC application script then SPI_CS is controlled from *smart*BASIC application allowing multi-dropping.
- SIO pin direction
  BL600 modules shipped from production with *smart*BASIC runtime engine FW, all SIO pins (with "default function" of "DIO") are mostly digital inputs (see Pin Definitions Table2). Remember to change the direction SIO pin (in your *smart*BASIC application script) if that particular pin is wired to a device that expects to be driven by the BL600 SIO pin configured as an output. Also these SIO pins that are inputs have by default (in FW) no internal pull-up or pull-down resistor-enabled, and therefore are floating. You are free to configure in your *smart*BASIC application script.

  Note: Internal pull-up, pull down will take current from VCC.

- nRESET pin (active low)
  Hardware reset. Wire out to push button or drive by host.
  By default module is out of reset when power applied to VCC pin.
- 50-Ohm RF track for interfacing with BL600-ST RF pin (pin 30)
  BL600-ST brings out the RF on trace pad (pin 30) and this must be tracked to–RSMA connector using 50-Ohms track on host PCB (to stay with regulatory certifications). More details in Checklist for PCB layout for BL600-ST.

6.2 PCB Layout on Host PCB - General

Checklist (for PCB)

- MUST locate BL600-Sx module close to the edge of PCB (mandatory for BL600-SA for on-board chips antenna to radiate properly).
- Use solid GND plane on inner layer (for best EMC and RF performance).
- Place GND vias close to module GND pads as possible
- Unused PCB area on surface layer can flooded with copper but place GND vias regularly to connect copper flood to inner GND plane. If GND flood copper underside the module then connect with GND vias to inner GND plane.
- Route traces to avoid noise being picked up on VCC supply and AIN(analogue) and SIO (digital) traces.
- Do NOT run any track near NC pins pin38 and 39 of BL600-Sx.
- Ensure no exposed copper underside of the module (refer to land pattern of BL600 development board).

6.3 PCB Layout on Host PCB for BL600-SA

6.3.1 Antenna keep-out on host PCB

The BL600-SA has an integrated chip antenna and its performance is sensitive to host PCB. It is critical to locate the BL600-SA on the edge of the host PCB (or corner) to allow the antenna to radiate properly. Refer to guidelines in section *PCB land pattern and antenna keep-out area for BL600-SA*. Some of those guidelines repeated below.

- Ensure there is no copper in the antenna keep-out area on any layers of the host PCB. Keep all mounting hardware and metal clear of the area to allow proper antenna radiation.

- For best antenna performance, place the BL600-SA module on the edge of the host PCB, preferably in the corner with the antenna facing the corner.
- The BL600 development board has the BL600-SA module on the edge of the board (not in the corner). The antenna keep-out area is defined by the BL600 development board which was used for module development and antenna performance evaluation is shown in Figure 10, where the antenna keep-out area is ~4.2 mm wide, 34.2 mm long; with PCB dielectric (no copper) height 1.539mm sitting under the BL600-SA antenna.
- A different host PCB thickness dielectric will have small effect on antenna.

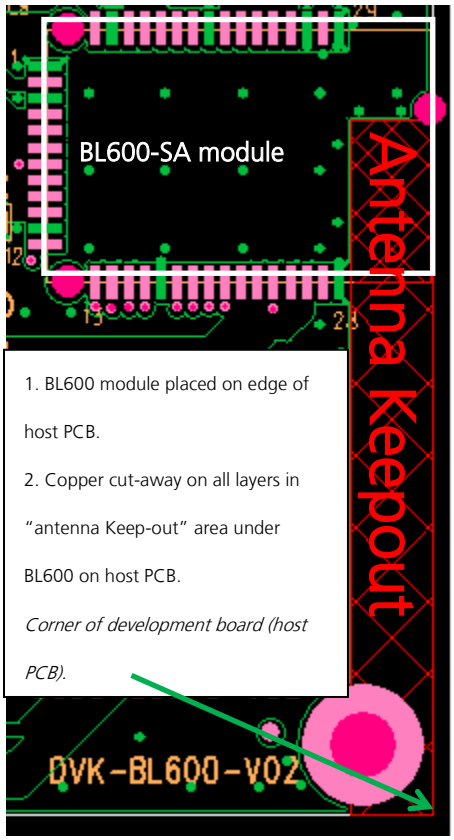


Figure 10: Antenna keep-out area (shown in red) used on the BL600 development board for BL600-SA module.

- The antenna-keep-out defined in the section *PCB land pattern and antenna keep-out area for BL600-SA* is for case when BL600-SA is placed in the corner of host PCB. When BL600-SA cannot be placed in corner of host PCB, then MUST place on the edge of the host PCB then cut-away copper (on all layers of host PCB) from the corner to the location of the BL600-SA antenna. For example Figure 10 shows what was done on the BL600 development board.

6.3.2 Antenna keep-out and Proximity to Metal or Plastic

Checklist (for metal /plastic enclosure)

- Minimum safe distance for metals without seriously compromising the antenna (tuning) is 40mm top/bottom and 30mm left or right.

- Metal close to the BL600-SA chip monopole antenna (bottom, top, left, right, any direction) will have degradation on the antenna performance. How much; that is entirely system dependent which means some testing by customer required (in their host application).
- Anything metal closer than 20mm will start to significantly degrade performance (S11, gain, radiation efficiency).
- It is best that the customer tests the Range with mock-up (or actual prototype) of the product to assess effects of enclosure height (and material whether metal or plastic).

6.4 50-Ohms RF trace on Host PCB for BL600-ST

Checklist (for PCB)

- RF_ANT pin (pin30) is on the BL600-ST module only. You MUST use a 50-Ohm trace from RF_ANT pin to RSMA RF antenna connector on host PCB.

Figure 11 shows the 10 mm length 50-Ohms RF trace (implemented as GCPW) from the BL600-ST module RF trace pads (GND, RF_ANT, GND) on BL600 development board.

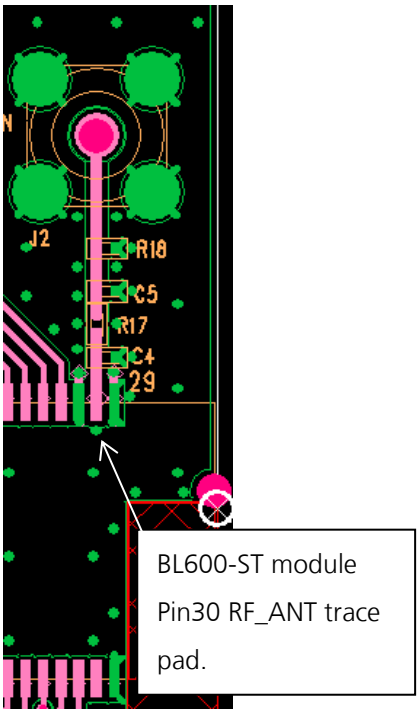


Figure 11: 50-Ohm trace design on BL600 development board (or host PCB) for use with BL600-ST module.

50-Ohms RF trace design and test verification for ensuring compliance

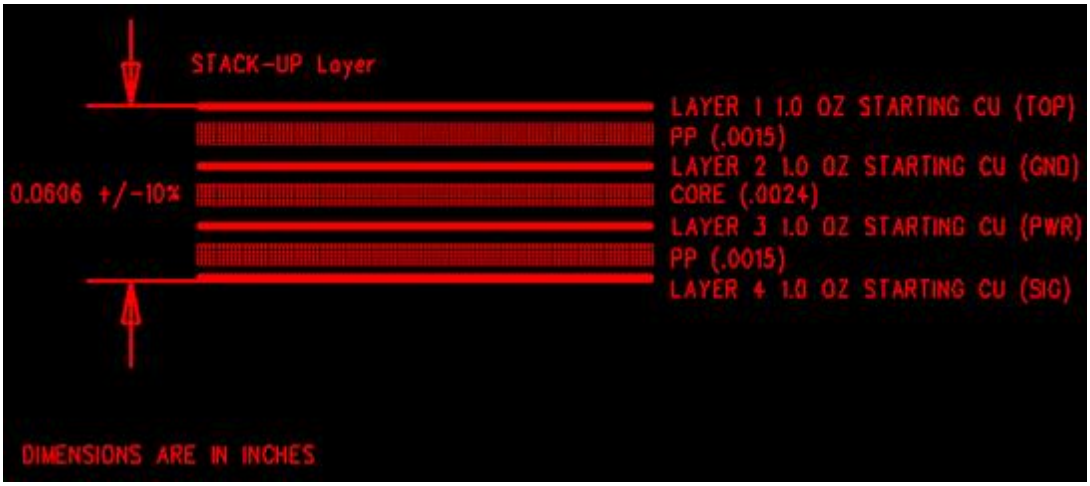
- Follow the 50-Ohms trace design used on the BL600 development board (PCB stack-up in Figure10). If this PCB-stack-up is not practical on customer design then design 50-Ohms for differing PCB stack-up.
- Use the same PCB material (FR4)
- The 50-Ohms trace should be controlled impedance trace e.g. ±10%.
- The 50-Ohms RF trace length should be 10mm (is recommended) as on the BL600 development board to reduce the trace length.

- Use the same 50-Ohms track width. BL600-ST module RF_ANT pad width is 0.5mm. Land pad is also 0.5mm. Therefore 50-Ohm RF trace width may be 0.5mm width. If 50-Ohm trace is wider, then a tapered section should be designed to gradually go from wider width to 0.5mm RF_ANT (land pad) width.
- Place GND vias regularly spaced either side of 50-Ohms trace to form GCPW (Grounded coplanar waveguide) transmission line.
- Use spectrum analyser to confirm the radiated (and conducted) signal is within the certification limit.

  To copy the BL600 development board 50-Ohms RF trace:

  - Use the same PCB material (FR4)
  - 0.5 mm track width
  - Use the same board L1 to L2 thickness (0.2032mm = 8Mil) for 50-Ohms impedance RF trace design.

    Place regular spaced through-hole GND vias (GCPW transmission line). BL600 development board uses 0.5mm diameter through-hole GND via with 2 to 4mm distance apart. Gap between RF_ANT trace and GND either side is 0.2 mm for below 50-Ohms impedance RF trace design.



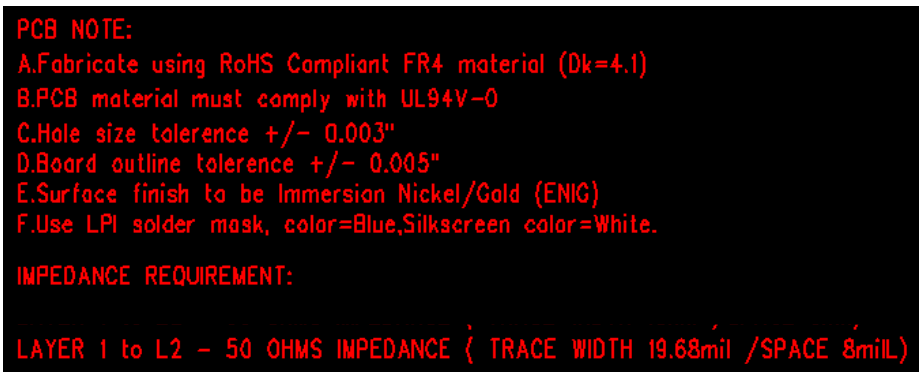


Figure 12: BL600 development board PCB stack-up and L1 to L2 50-Ohms impedance RF trace design.

6.5 External Antenna Integration with BL600-SC and BL600-ST

Please refer to the regulatory sections for FCC, IC, CE, and Japan for details of use of BL600-Sx with external antennas in each regulatory region.

The BL600 family has been designed to operate with the below external antennas (with a maximum gain of 2.21 dBi). The required antenna impedance is 50 ohms.

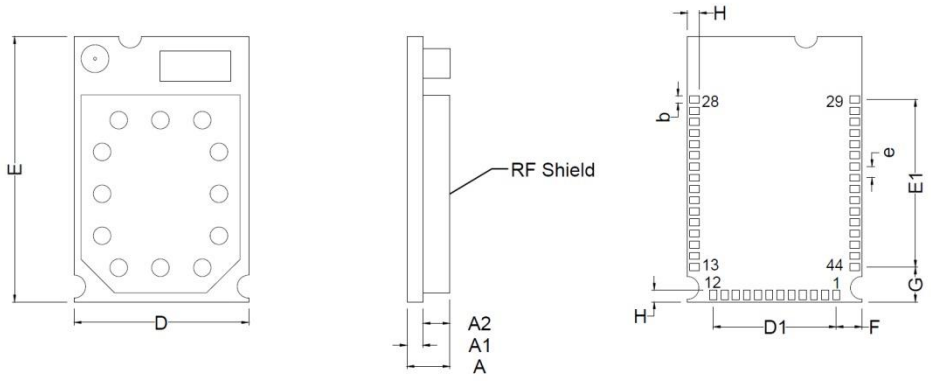
External antennas better radiation efficiency.

External Antenna Part Number	Mfg.	Type	Gain (dBi)	Connector Type	BL600 Part number
EDA-8709-2G4C1-B27-CY	MAG. Layers	Dipole	2.0	IPEX-4 Note1	BL600-SC
PCA-4606-2G4C1-A33-CY	MAG. Layers	PCB Dipole	2.21	IPEX-4 Note1	BL600-SC
EDA-8709-2G4R2-A40-CY	MAG. Layers	Dipole	2.0	R-SMA Male	BL600-ST

Note 1: Integral RF co-axial cable (1.13 mm OD) with length 100±5 mm with IPEX-4 compatible connector.
Antenna manufacturer Mag-Layers contact information:
Sales: Croyee Tai
Tel: 886-3-597-2488 #250
Email: croyeetai@maglayers.com.tw

7 MECHANICAL DETAILS

7.1 BL600 Mechanical Details



Description	BL600			
Size	19 x 12.5 x 3.05mm			
Pitch	.8mm			
Dimension	Minimum	Typical	Maximum	Notes
A	3.05	3.16	3.27	
A1	1.06	1.16	1.26	PCB Thickness
A2	1.99	2	2.01	RF Shield Height
b	.45	.5	.55	Global pad width
D	12.4	12.5	12.6	
E	18.9	19	19.1	
e		.8		Global pitch
D1		8.8		
E1		12		
F		1.85		Pad Center to Board edge
G		2.50		Pad Center to Board edge
H		.85		Global length of pad to edge of board
Units	mm			

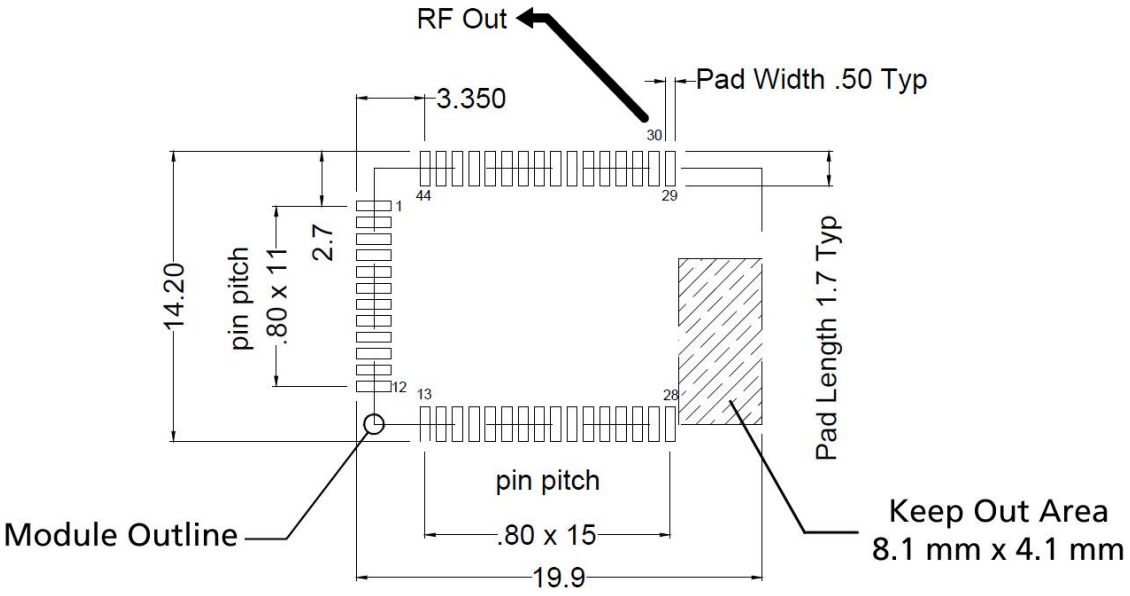
Title: Module Package Dimensions			
TOLERENCE UNLESS STATED		MATERIAL	DRAWN: D Chapman
x +/-0.3	x.xx +/-0.03	FINISH	CHECKED
x.x+/-0.1		COLOUR	APPROVED
DIMENSIONS IN MM UNLESS STATED	SCALE	THIRD ANGLE PROJECTION	DWG No: BL600 Page 1of 2
PROJECT: BL600			

Figure 13: BL600 Mechanical drawings

Development Kit Schematics can be accessed here from the *Documentation* tab :-

http://lairdtech.com/Products/Embedded-Wireless-Solutions/Bluetooth-Radio-Modules/BL600-Series/

7.2 PCB Land Pattern and Antenna Keep-out for BL600-SA



Dimensions in mm.

APPLICATION NOTES

1. "RF Out" on pin30 is for BL600-ST only. BL600-ST brings out the RF on trace pad (pin 30) and this MUST be tracked with a 50-Ohms RF transmission line (preferably GCPW) on the customers host PCB. More details in section *50-Ohms RF trace on Host PCB for BL600-ST.*
2. Ensure there is no copper in the antenna 'keep out area' on any layers of the host PCB. Also keep all mounting hardware or any metal clear (Refer to 6.3.2) on of the area to reduce effects of proximity detuning the antenna and to help antenna radiate properly.
3. For BL600-SA (has on-board chip antenna) best antenna performance, the module BL600-SA MUST be placed on the edge of the host PCB and preferably in the **corner** with the antenna facing the corner. **Above "Keep Out Area" is the module placed in corner of PCB.** If BL600-SA is not placed in corner but on edge of host PCB, the antenna "Keep Out Area" is extended (see Note4).
4. BL600 development board has BL600-SA placed on the edge of the PCB board (and not in corner) for that the Antenna keep out area is extended down to the corner of the development board, see section *PCB Layout on Host PCB for BL600-SA*, Figure10. This was used for module development and antenna performance evaluation.
5. Ensure no exposed copper under module on host PCB.
6. The user may modify the PCB land pattern dimensions based on their experience and / or process capability.

8 Application Note for Surface Mount Modules

8.1 Introduction

Laird Technologies surface mount modules are designed to conform to all major manufacturing guidelines. This application note is intended to provide additional guidance beyond the information that is presented in the User Manual. This Application Note is considered a living document and will be updated as new information is presented.

The modules are designed to meet the needs of a number of commercial and industrial applications. They are easy to manufacture and conform to current automated manufacturing processes.

8.2 Shipping

Modules are shipped in ESD (Electrostatic Discharge) safe trays that can be loaded into most manufacturers pick and place machines. Layouts of the trays are provided in Figure 8-1.

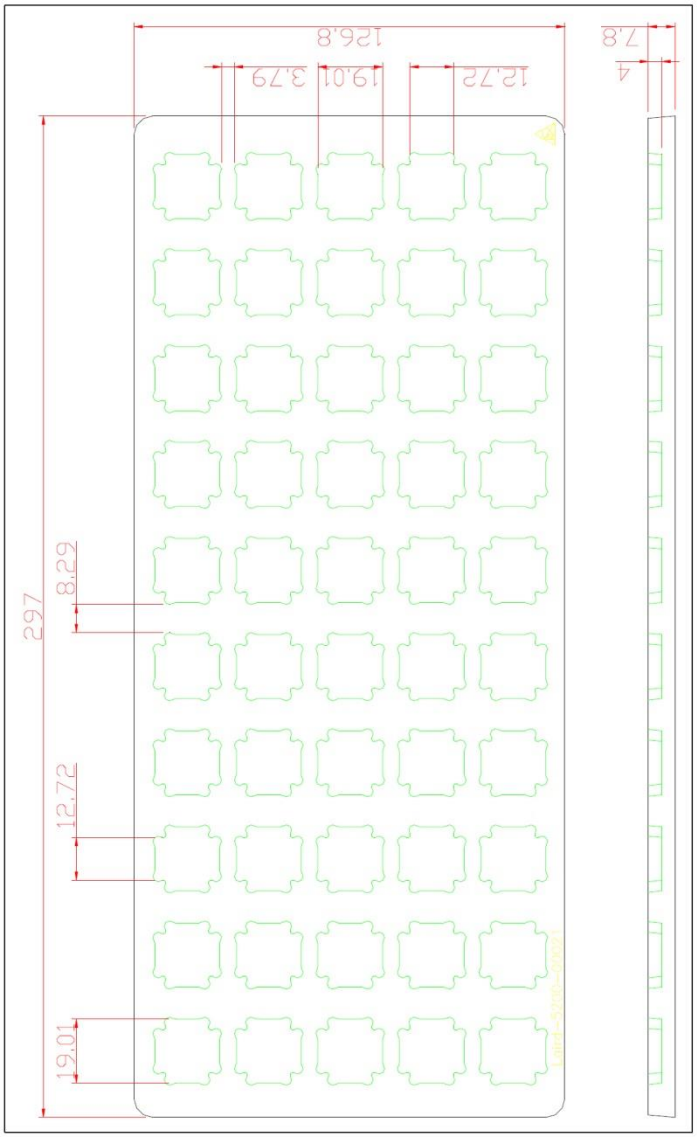


Figure 8-1: BL600 Shipping Tray Details

8.3 Reflow Parameters

Laird Technologies surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Laird Technologies' surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

Important: During reflow, modules should not be above 260° and not for more than 30 seconds.

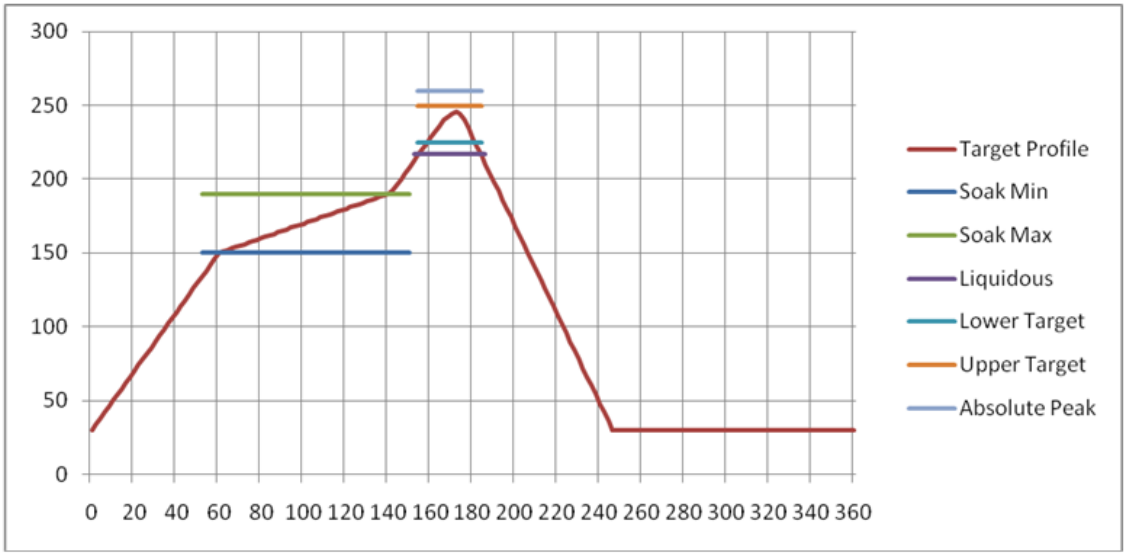


Figure 8-2: Recommended Reflow Temperature

Temperatures should not exceed the minimums or maximums presented in Table 9.

Table 9: Recommended Maximum and minimum temperatures

Specification	Value	Unit
Temperature Inc./Dec. Rate (max)	1~3	°C / Sec
Temperature Decrease rate (goal)	2-4	°C / Sec
Soak Temp Increase rate (goal)	.5 - 1	°C / Sec
Flux Soak Period (Min)	70	Sec
Flux Soak Period (Max)	120	Sec
Flux Soak Temp (Min)	150	°C
Flux Soak Temp (max)	190	°C
Time Above Liquidous (max)	70	Sec
Time Above Liquidous (min)	50	Sec
Time In Target Reflow Range (goal)	30	Sec
Time At Absolute Peak (max)	5	Sec
Liquidous Temperature (SAC305)	218	°C
Lower Target Reflow Temperature	240	°C
Upper Target Reflow Temperature	250	°C
Absolute Peak Temperature	260	°C

9 FCC AND IC REGULATORY STATEMENTS

Model	US/FCC	CANADA/IC
BL600-SA	PI4BL600	1931B-BL600
BL600-SC	PI4BL600	1931B-BL600
BL600-ST	PI4BL600T	1931B-BL600T

Important: The BL600-ST holds a limited modular approval for the U.S and Canada markets. To ensure regulatory compliance when integrating the BL600-ST into a host device, it is necessary to follow the design implementation requirements in this manual so the BL600-ST modular certification can carry over to the host device. The RF trace path from the BL600-ST to the approved antenna must be equivalent to what was approved for use by Laird. If these layout requirements cannot be met, the OEM will need to either seek a new FCC/ IC approval for their device or seek a Class 2 Permissive Change through Laird Technologies which adds the new antenna layout to the BL600-St approval. Contact Laird Technologies for further guidance.

The BL600-SA and BL600-SC hold full modular approvals. The OEM must follow the regulatory guidelines and warnings listed below to inherit the modular approval.

PART #	FORM FACTOR	TX OUTPUT	ANTENNA
BL600-SA-XX	Surface Mount	4dBm	Ceramic
BL600-SC-XX	Surface Mount	4dBm	IPEX MHF4
BL600-ST-XX	Surface Mount	4dBm	Trace Pad
*Last two slots "XX" in Part # are used for production firmware release changes. Can be values 01-99, aa-zz			

The BL600 family has been designed to operate with the antennas listed below with a maximum gain of 2.21 dBi. The required antenna impedance is 50 ohms.

Item	Part Number	Mfg.	Type	Gain (dBi)	Model
1	AT5020-E3R0HBANT/LF	ACX	Ceramic	0	BL600-SA
2	EDA-8709-2G4C1-B27-CY	MAG. Layers	Dipole	2.0	BL600-SC
3	PCA-4606-2G4C1-A33-CY	MAG. Layers	Dipole	2.21	BL600-SC
4	EDA-8709-2G4R2-A40-CY	MAG. Layers	Dipole	2.0	BL600-ST

Note: The OEM is free to choose another vendor's antenna of like type and equal or lesser gain as an antenna appearing in the table and still maintain compliance. Reference FCC Part 15.204(c)(4) for further information on this topic.

To reduce potential radio interference to other users, the antenna type and gain should be chosen so that the equivalent isotropic radiated power (EIRP) is not more than that permitted for successful communication.

9.1 Power Exposure Information

Federal Communication Commission (FCC) Radiation Exposure Statement:
This EUT is in compliance with SAR for general population/uncontrolled exposure limits in ANSI/IEEE C95.1-1999 and had been tested in accordance with the measurement methods and procedures specified in OET Bulletin 65 Supplement C.

This transceiver must not be co-located or operating in conjunction with any other antenna, transmitter, or external amplifiers. Further testing / evaluation of the end product will be required if the OEM's device violates any of these requirements.

The BL600 is fully approved for mobile and portable applications.

9.2 OEM Responsibilities

WARNING: The OEM must ensure that FCC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Laird Technology FCC identifier for this product.

Contains FCC ID: PI4xxxxx IC: 1931B-xxxxx

If the size of the end product is larger than 8x10cm, then the following FCC part 15.19 statement has to also be available on visible on outside of device:

The enclosed device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation

Label and text information should be in a size of type large enough to be readily legible, consistent with the dimensions of the equipment and the label. However, the type size for the text is not required to be larger than eight point.

CAUTION: The OEM should have their device which incorporates the BL600 tested by a qualified test house to verify compliance with FCC Part 15 Subpart B limits for unintentional radiators.

CAUTION: Any changes or modifications not expressly approved by Laird Technology could void the user's authority to operate the equipment.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does not cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to correct the interference by one or more of the following measures:

- Re-orient or relocate the receiving antenna
- Increase the separation between the equipment and the receiver
- Connect the equipment to an outlet on a circuit that is different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Warning:

"THIS DEVICE COMPLIES WITH PART 15 OF THE FCC RULES AND INDUSTRY CANADA LICENSE-EXEMPT RSS STANDARD(S). OPERATION IS SUBJECT TO THE FOLLOWING TWO CONDITIONS: (1) THIS DEVICE MAY NOT CAUSE HARMFUL INTERFERENCE, AND (2) THIS DEVICE MUST ACCEPT ANY INTERFERENCE RECEIVED, INCLUDING INTERFERENCE THAT MAY CAUSE UNDESIRED OPERATION.

Industry Canada (IC) Warning:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

French equivalent is:

Le présent appareil est conforme aux CNR d'Industrie Canada applicable aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

IC Radiation Exposure Statement

This EUT is compliance with SAR for general population/uncontrolled exposure limits in IC RSS-102 and had been tested in accordance with the measurement methods and procedures specified in IEEE 1528.

REMARQUE IMPORTANTE

Déclaration IC d'exposition aux radiations
Ce EUT est conforme avec SAR pour la population générale / limites d'exposition non contrôlée à IC RSS-102 et a été testé en conformité avec les méthodes de mesure et procédures spécifiées dans la norme IEEE 1528.

Modular Approval

OEM integrator is still responsible for testing their end product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

Approbation modulaire

OEM intégrateur est toujours responsable de tester leur produit final pour les exigences de conformité supplémentaires nécessaires à ce module installé (par exemple, les émissions de périphériques numériques, les exigences de périphériques PC, etc.)

IMPORTANT NOTE:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: " BL600-SA & BL600-SC Contient des IC: 1393-BL600"; BL600-ST Contient des IC: 1393-BL600T"

10 JAPAN (MIC) REGULATORY

The BL600 is approved for use in the Japanese market. The part numbers listed below hold WW type certification. Refer to ARIB-STD-T66 for further guidance on OEM's responsibilities.

Model	Certificate Number	Antenna
BL600-SA	204-320049	Ceramic
BL600-SC	204-320050	IPEX MHF4
BL600-ST	204-320048	Trace Pad

10.1 Antenna Information

The BL600 was tested with antennas listed below. The OEM can choose a different manufacturers antenna but must make sure it is of same type and that the gain is lesser than or equal to the antenna that is approved for use.

Item	Part Number	Mfg.	Type	Gain (dBi)	Model
1	AT5020-E3R0HBANT/LF	ACX	Ceramic	0	BL600-SA
2	EDA-8709-2G4C1-B27-CY	MAG. Layers	Dipole	2.0	BL600-SC
3	PCA-4606-2G4C1-A33-CY	MAG. Layers	Dipole	2.21	BL600-SC
4	EDA-8709-2G4R2-A40-CY	MAG. Layers	Dipole	2.0	BL600-ST

11 CE REGULATORY

The BL600-SA / BL600-SC / BL600-ST have been tested for compliance with relevant standards for the EU market. The BL600-SC and BL600-ST modules were tested with a 2.21 dBi antenna. The OEM can operate the BL600-SC and BL600-ST modules with any other type of antenna but must ensure that the gain does not exceed 2.21 dBi to maintain the Laird Technologies approval.

The OEM should consult with a qualified test house before entering their device into an EU member country to make sure all regulatory requirements have been met for their complete device.

Reference the Declaration of Conformities listed below for a full list of the standards that the modules were tested to. Test reports are available upon request.

11.1 Antenna Information

The antennas listed below were tested for use with the BL600. For CE mark countries, the OEM is free to use any manufacturer's antenna and type of antenna as long as the gain is less than or equal to the highest gain approved for use (2.21dBi) Contact a Laird Technologies representative for more information regarding adding antennas.

Item	Part Number	Mfg.	Type	Gain (dBi)	Model
1	AT5020-E3R0HBANT/LF	ACX	Ceramic	0	BL600-SA
2	EDA-8709-2G4C1-B27-CY	MAG. Layers	Dipole	2.0	BL600-SC
3	PCA-4606-2G4C1-A33-CY	MAG. Layers	Dipole	2.21	BL600-SC
4	EDA-8709-2G4R2-A40-CY	MAG. Layers	Dipole	2.0	BL600-ST

Note: The BL600 module internal BLE chipset IC pins are rated 4 kV (ESD HBM). ESD can find its way through the external JTAG connector (if used on the customers design), if discharge is applied directly. Customer should ensure adequate protection against ESD on their end product design (using the BL600 module) to meet relevant ESD standard (for CE, this is EN301-489).

12 EU DECLARATIONS OF CONFORMITY

12.1 BL600-SA / BL600-SC / BL600-ST

Manufacturer:	Laird
Product:	BL600-SA, BL600-SC, BL600-ST
EU Directive:	RTTE 1995/5/EC
Conformity Assessment:	Annex IV

Reference standards used for presumption of conformity:

Article Number	Requirement	Reference standard(s)
3.1a	Health and Safety	EN60950-1:2006+A11:2009+A1:2010+A12:2011
3.1b	Protection requirements with respect to electromagnetic compatibility	EN 301 489-1 V1.9.2 (2011-09) EN 301 489-17 V2.2.1 (2012-09) Emissions: EN55022:2006/A1:2007 (Class B) Immunity: EN61000-4-2:2009 EN61000-4-3:2006/A1:2008/A2:2010
3.2	Means of the efficient use of the radio frequency spectrum	EN 300 328 V1.8.1 (2012-06)

Declaration:

We, Laird, declare under our sole responsibility that the essential radio test suites have been carried out and that the above product to which this declaration relates is in conformity with all the applicable essential requirements of Article 3 of the EU Directive 1999/5/EC, when used for its intended purpose.

Place of Issue:	Laird Saturn House, Mercury Park Wooburn Green HP100HH, United Kingdom tel: +44 (0)1628 858 940 fax: +44 (0)1628 528 382
Date of Issue:	April2013
Name of Authorized Person:	Andrew Dobbing, Engineering Manager
Signature:	

13 ORDERING INFORMATION

part number	DESCRIPTION
BL600-SA	Single Mode BLE Module featuring *smart*BASIC – integrated antenna
BT730-SC	Single Mode BLE Module featuring *smart*BASIC – IPEX MHF4 connector
BL600-ST	Single Mode BLE Module featuring *smart*BASIC – Trace Pad
DVK – BL600-SA	Development board with BL600-SA module soldered in place
DVK – BL600-SC	Development board with BL600-SC module soldered in place
DVK – BL600-ST	Development board with BL600-ST module soldered in place

13.1 General Comments

This is a preliminary datasheet. Please check with Laird for the latest information before commencing a design. If in doubt, ask.

14 BLUETOOTH SIG APPROVALS

14.1 End Product Listings (EPLs)

This section covers the procedure for generating a new EPL (End Product Listing), on the Bluetooth SIG website. In the instance of a Bluetooth End Product design, a member can create their own EPL which will have a direct reference to the original Bluetooth End Product QDID.

BL600 Original End Product listing

Design Name	Owner	QDID number	Link to listing on the SIG website
BL600 Module	Laird Technologies	B020700	BL600 Module listing

The BL600 Module incorporates the following Bluetooth components from Nordic Semiconductor ASA;

Design Name	Owner	QDID number	Link to listing on the SIG website
nRF51XXX_RF	Nordic Semiconductor ASA	B020553	nRF51XXX_RF
nRF51xxx - S110 link layer	Nordic Semiconductor ASA	B020269	nRF51xxx - S110 link layer listing
nRF51xxx - S110 host	Nordic Semiconductor ASA	B020552	nRF51xxx - S110 host listing

Assumptions

This procedure assumes that the member is using the original Bluetooth End Product design with no modifications. The original Bluetooth End Product design includes all the mandatory protocol and profiles layers. You can generate a new EPL (End Product Listing) by using the web interface on the Bluetooth SIG website. Figure 3 shows the basic concept of how an EPL is referenced back to a Bluetooth End Product.

Figure 3: EPL referenced back to BT end product

The following link provides an overview of the EPL system:

https://www.bluetooth.org/technical/qualification/eploverview.htm

For a detailed procedure of how to make an EPL entry, please refer to the following SIG document;

https://www.bluetooth.org/docman/handlers/DownloadDoc.ashx?doc_id=71880

Note: Alternatively the member can choose to have a new QDID for their own End Product Design if they do not want any reference the original QDID listing. However it should be noted that this would incur a listing fee, please refer to FAQ 214 below.

Useful FAQ links

https://www.bluetooth.org/ticketing/view_article.cfm?action=article_comment&aid=275

https://www.bluetooth.org/ticketing/view_article.cfm?action=article_comment&aid=214

https://www.bluetooth.org/ticketing/view_article.cfm?action=article_comment&aid=112

Additional Assistance

Please contact your local sales representative for further assistance

Laird is the world leader in the design and manufacture of customized, performance-critical products for wireless and other advanced electronics applications.

Laird Technologies partners with its customers to find solutions for applications in various industries such as:

- Network Equipment
- Telecommunications
- Data Communications
- Automotive Electronics
- Computers
- Aerospace
- Military
- Medical Equipment
- Consumer Electronics

Laird offers its customers unique product solutions, dedication to research and development, as well as a seamless network of manufacturing and customer support facilities across the globe.

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LWS-UM-BL600-Sx